

Abstract of the Disclosure

[00100] A SRAM cell includes double-gated PMOS and NMOS transistors to form a latch and retain a value. The unique MOSFET transistor architecture provides a four terminal device for independent gate control, a floating body device, and a dynamic threshold device. The channel may have a U-shaped cross-sectional area to increase the channel length and gate control. First and second insulating spacers are disposed on opposing sides of the top gate such that the first spacer is between the source and the top gate, and the second spacer is between the drain and the top gate. The source and drain include extensions that extend proximate to the spacers and couple to the channel. The spacers shield the channel from the field effect of the source and drain, and further resist compression of the channel by the source and drain.